

With a scalable solution from Agilent Technologies, design team members can customize product offerings to meet their unique requirements. Solutions range from emulation probes combined with the industry's leading debuggers to emulation with real-time trace to solve today's most complex Motorola MPC82XX design problems. Agilent's solutions are designed to meet your needs today and protect your investment as your needs change in the future. With logic analysis providing timing and state analysis, you can monitor microprocessor activity in relation to other important system signals such as a PCI bus, other microprocessors, I/O devices or ATM and Ethernet ports. Traditional emulation systems don't allow you to time-correlate events across your entire system using timing, analog, and state analysis for your most difficult integration prob-

The logic analyzer is nonintrusive, allowing you to run your target system at full speed. A system trace, up to 32 M deep, can be combined with complex triggering to find the toughest problems. The microprocessor instruction set execution can be correlated to high-level source code with the source correlation tool set.



**Agilent Technologies** Innovating the HP Way

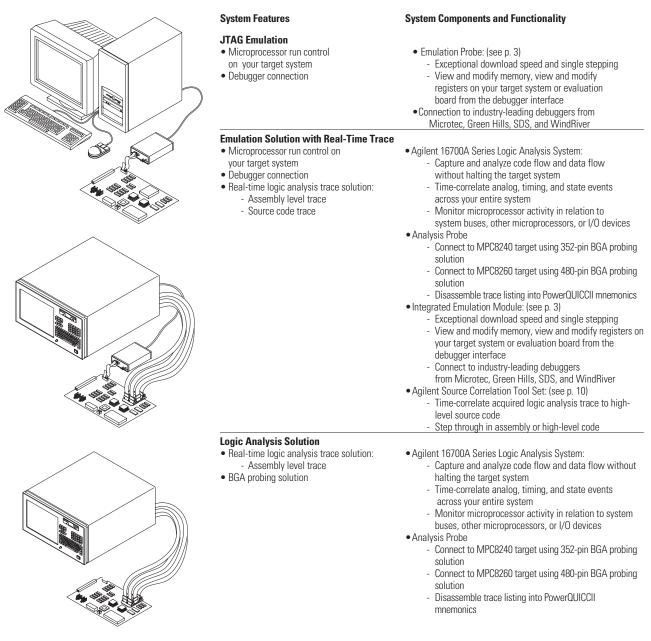
## **Agilent Technologies' Scalable Solutions**

Agilent's emulation and logic analysis solutions are scalable for each member of the digital design team. The following are three typical configurations for firmware/ software debug, hardware debug, and system integration.

Components of these solutions include a logic analyzer, emulation

probe/module, analysis probe, inverse assembler, source correlation tool set, and system performance analysis tool set.

Information on each of these components is included in this document.



Microprocessor	Package Type	Bus Speed	JTAG Emulation	Emulation Solution with Real-Time Trace	Logic Analysis Solution
MPC8260	BGA	Up to 66 MHz	Х	x	х
MPC8240	BGA	Up to 100 MHz	Х	Х	Х

Table 1: Emulation and Analysis Solutions for PowerQUICC II Microprocessors

# **Emulation Probe and Module**

The emulation probe and module provide the same functionality. The emulation probe is a standalone product, as shown in figure 1. The emulation module is an integrated plug-in for the Agilent 16700A Series logic analysis systems.

The emulation probe and module have been improved to provide exceptional download speed and single stepping. These improvements include:

- 32 bit microprocessor
- 100 Base TX LAN
- New scan-chain controller

Both the probe and module help you debug your code by providing run control, code download, and memory/register display and modification. You can control program execution through single stepping, run/break, and set/modify breakpoints. You can also run code at full speed in the target. Agilent's new emulation probes now allow you to complete these tasks more quickly so you can bring your products to market sooner.

An industry leading debugger can be used to control both the emulation probe and module. Alternatively, they can be controlled by the emulation control interface provided with the logic analyzer. These interfaces are described on page 4.

The emulation probe and module can be controlled over your local area network (LAN) by the debugger and connect to your target through a 16-pin Berg style connector, as shown in figure 4.

Unlike traditional emulators, the emulation probes and modules provide more stable operation by accessing only the debug pins of the microprocessor. You don't need a serial port on your target system to download code. Unlike ROM monitors, they don't require user memory.

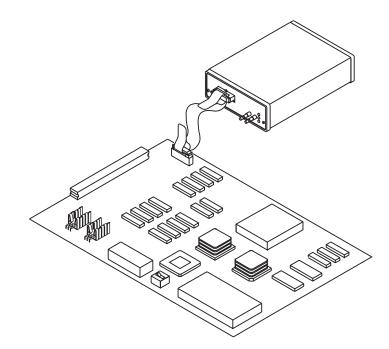


Figure 1: Standalone Emulation Probe

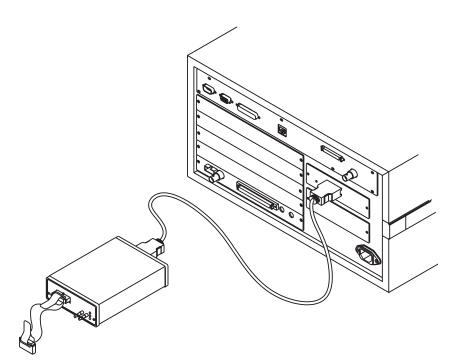


Figure 2: 16702A Logic Analysis System with Integrated Emulation Module

#### **Debugger Interface**

Industry-leading debuggers can control the emulation probe and module. You can set breakpoints, single-step through code, examine variables, and modify source code variables from the high-level source code debugger interface.

Debugger interfaces must be ordered directly from the debugger vendor.

#### **Debugger Connections**

Green Hills Software, Inc. 30 West Sola Street Santa Barbara, CA 93101 USA Phone: (805) 965-6044 http://www.ghs.com

Microtec, A Mentor Graphics Company 880 Ridder Park Drive San Jose, CA 95131 USA Phone: (800) 950-5554 Phone: (408) 487-7000 http://www.mentor.com/microtec

Diab-SDS 323 Vintage Park Drive Foster City, CA 94404 USA Phone: 630-724-2520 http://www.diabsds.com

WindRiver Systems 500 Wind River Way Alameda, CA 94501 USA Phone: 1-800-545-WIND http://www.wrs.com

Please check with your local Agilent Test and Measurement sales office or visit our web site at http://www.agilent.com/find/las-data for the current list of debugger connections.

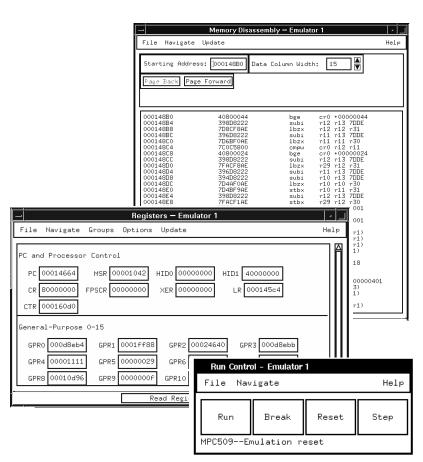


Figure 3: Emulation Control Interface

## **Emulation Control Interface**

The emulation module integrated into the logic analysis system can be controlled directly by the emulation control interface. You can easily display and modify contents of microprocessor registers, system memory, and I/O. You can also view memory code segments disassembled into familiar Motorola MPC82XX assembly instructions.

From the run control window you can instruct the microprocessor to run, break, reset, or single-step. You also can choose whether the memory, I/O, and register displays are updated for breaks and single steps. Writing command files that set up registers, memory, and I/O in your system is easy with the command language. Once the command file is written, save it on the logic analyzer hard disk. When you want to initialize your hardware system to a particular state, simply recall and execute the command file. Unlike a debugger interface, the emulation control interface does not reference back to the high-level source code.

# Emulation Module and Probe Migration

Agilent Technologies protects your current investment by providing a migration path for the emulation modules and probes as your needs change. To move from one processor family to another, simply order a migration kit for the emulation module or probe, which will provide all the necessary hardware, firmware, and cables to support your new processor family at a fraction of the cost of a new system.

This same migration path works for the emulation probes or emulation modules. Migration is available for those processors in the E5900B Series.

# Emulation Module Triggering Integration with Logic Analyzer

With the emulation module, use the powerful triggering of the 16700A Series logic analysis systems to halt on events such as microprocessor activity, system buses, or other external events. The emulation module also can trigger the logic analyzer when a breakpoint is hit. This provides powerful event correlation between the debugger interface environment and the logic analyzer.

Specification	Description	
Microprocessors	Motorola MPC82	260 PowerQUICC II, MPC8240
Supported		
External Bus Speed	66 MHz / 100 MI	Hz
Physical Connections	Ethernet	Autosensing 10/100 Ethernet
	RS-232-C	9600 Kbaud rate
Number of Breakpoints	Virtually unlimite	ed software breakpoints
	or one hardware	breakpoint
Physical Size	105 mm width x	151 mm depth x 40 mm height
Environmental		
Temperature	Operating: 5 °C t	to +40 °C (+41 °F to + 104 °F)
	Nonoperating:	40 °C to +70 °C (–40 °F to +158 °F)
Altitude	Operating: 4,600	m (15,000 ft)
	Nonoperating: 4,	600 m (15,000 ft)
Humidity	15% to 80% @ 4	10 °C for 24 hours
<b>Regulatory Compliance</b>	EMC CISPR 11:	:1990/EN 55011:1991 Group 1, Class A
	IEC 801-2:1991/E	EN 50082-1:1992 4 kV CD, 8 kV AD
	IEC 801-3:1984/E	EN 50082-1:1992 3 V/m, (1 kHz 80% AM, 27-1 kMz )
	IEC 801-4: 1988 /	/ EN 50082-1:1992 0.RkV Sig lines, 1 kV Power lines
Safety Approvals	IEC 1010-1:1990	
	AMD 1:1992	
	UL 1244	
	CSA-C22.2 No. 2	31

Table 2: Emulation Probe and Module Specifications

## Emulation Probe and Module Target Connection Information

A 2x8 0.1 inch center BERG-style connector is required to connect the emulation probe to the JTAG interface for the MPC8260 or the MPC8240. The header should be placed as close to the microprocessor as possible to ensure signal integrity. TDO, TDI, TCK, TMS, and TRST should have signal traces less than three inches between the JTAG connector and the microprocessor. The PowerQUICC II must be the only device on the JTAG scan chain. These signals are sensitive to cross-talk and cannot be routed next to active signals such as clocks.

The TDI, TCK, TMS, and TRST signals must not be actively driven by the target system when the debug port is being used.

The Agilent emulation probe/module adds about 40pF to all target system signals routed to the debug connector. This added capacitance may reduce the rise time of the HRESET and SRESET signals beyond the processor specifications. If so, the target may need to increase the pull-up current on these signal lines.

When the 'rst' command on the probe/module is used, HRESET is held low for approximately 300ms. Realtime trace analysis consists of a physical connection to signals on the Motorola MPC82XX microprocessors, acquisition of relevant data, and analysis of the real-time captured bus information.

Physical connection to the microprocessor is provided by an AMP Mictor probing solution.

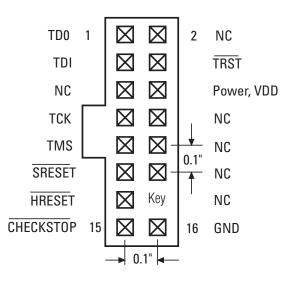


Figure 4: Target Development Board Header Connector (Top View)

Header Pin No.	MPC 82XX I/O	Signal Name	Resistor	
1	Out	TD0		
2		NC		
3	In	TDI	1K $\Omega$ pulldown	
4	ln	TRST	10K $\Omega$ pullup	
5		NC		
6		Power*	1K $\Omega$ series	
7	In	ТСК	10K $\Omega$ pullup	
8		NC		
9	In	TMS	10K $\Omega$ pullup	
10		NC		
11	ln	SRESET	10K $\Omega$ pullup	
12		NC		
13	In	HRESET	10K $\Omega$ pullup	
14		KEY		
15	Out	CHECKSTOP	1KΩ pullup	
16		GND		

Table 3. JTAG Interface Connections

	*The +POWER signal is sourced from the development board and is used as a
	reference signal. It should be the power signal supplied
	to the processor (either +3.3V or +5V). It does not supply power to the emulation
	probe.
Note:	NC Refers to No Connect

Notes and Information:

If the target board does not use the QACK signal, the board must have a pulldown
resistor to pull this signal low. This allows the PowerPC to enter the state required for reading and writing
processor scan string data.

## **Reset Signals for the MPC8240**

The SRESET, HRESET signals from the JTAG connector may be logically ORed with their respective signals on the target system. The MPC8240 has two hard resets, HRST\_CPU and HRST\_CTRL. HRESET from the debug connector must be routed to the HRST\_CPU reset logic and optionally routed to the HRST\_CTRL reset logic depending on system requirements.

The emulation probe/module drives SRESET and HRESET with open-drain drivers using 2.7 Kohm pullups to VDD. The target system designer can take advantage of these open-drain drivers by wire-ORing SRESET and/or HRESET to open-drain drivers on the target system. It is not necessary to use a wire-OR configuration, but reset status messages can only be generated by the probe/module when using the wire-ORed configuration.

The TRST signal from the JTAG connector must be logically ORed with TRST on the target system. TRST is actively driven by the probe/module and can not be wire-ORed.

#### **Reset Signals for the MPC8260**

SRESET and HRESET from the debug connector may be ORed with the respective SRESET and HRESET signals on the target system. They can be logically ORed or wire-ORed on the target system. The emulation probe/module drives SRESET and HRESET with open-drain drivers using 2.7 Kohm pullups to VDD.

It is not necessary to use a wire-OR configuration, but reset status messages can only be generated by the probe/module when using the wire-ORed configuration.

The TRST signal from the JTAG connector must be logically <u>ORed</u> with TRST on the target system. TRST is actively driven by the probe/module and cannot be wire-ORed.

# **Real-Time Trace Analysis**

Real-time trace analysis consists of a physical connection to signals on the Motorola MPC8260 and MPC8240 microprocessors, acquisition of relevant data, and analysis of the real-time captured bus information. Physical connection to the microprocessor is provided by an AMP Mictor probing solution.

The real-time trace analysis solutions for the Motorola MPC82XX include inverse assembly, source correlation, and system performance analysis. For information on the data acquisition modules for the 16700A Series logic analysis systems, please refer to related literature on page 34.

MPC82XX Microprocessor	Supported Speed	Probing Solutions	Real-Time Trace Solutions
MPC8260	Up to 66 MHz external bus speed	<ul> <li>Analysis Probe:</li> <li>MPC8240 352-pin BGA probing solution</li> <li>MPC8260 480-pin BGA probing solution</li> <li>Inverse assembler included</li> <li>Access to all microprocessor</li> </ul>	<ul> <li>Inverse Assembly:</li> <li>Disassembly of bus information into MPC82XX microprocessor mnemonics</li> <li>MPC82XX configuration files for logic analyzer</li> </ul>
MPC8240	Up to 100 MHz external bus speed	<ul> <li>Access to an introprocession signals for logic analysis</li> <li>Optional Mictor Connector Solution:</li> <li>Mictor connectors designed in target for access to critical signals for logic analysis</li> </ul>	Source Correlation: • Time-correlation of acquired trace to high-level source code • Trigger and search through trace in high-level source code
			System Performance Analysis: • Statistical performance measurements on trace data • State overview, state interval, time interval, and time overview measurements

Table 4: Real-Time Trace and Probing Alternatives

# MPC8260 PowerQUICC II

Supported Memory Modes	Unsupported Memory Modes
<ul> <li>GPCM, UPM, and SDRAM memory controllers</li> </ul>	Local-bus
External L2-cache fills	
PCI bus	

## **MPC8240**

Supported Memory Modes	
<ul> <li>SDRAM, Flash, SRAM, DRAM</li> </ul>	
PCI bus	

#### **Inverse Assemblers**

The inverse assemblers quickly configure the logic analyzers by labeling address, data, and status signals for the MPC8240 or the MPC8260 microprocessors. They also provide processor mnemonics in the trace listing for easy correlation between captured data and target code. The inverse assemblers work with the Agilent B4620B source correlation tool set to provide time correlation between the assemblylevel trace and the high-level source code.

The inverse assemblers provide filters and color coding to show and/or suppress different instructions such as data reads, data writes, unexecuted prefetches, and memory map regions.

The inverse assemblers have several modes of operation, depending on your microprocessor configuration. The inverse assemblers provide PowerQUICC II mnemonics, but the cache must be off to see all cycles on the microprocessors.

The MPC8240 inverse assembler has a code-flow only mode which requires only 68-channels of logic analysis. The opcodes are retrieved from an S-record file instead of the data bus, cutting the required channel count in half. An additional logic analyzer module can easily be added for data visibility.

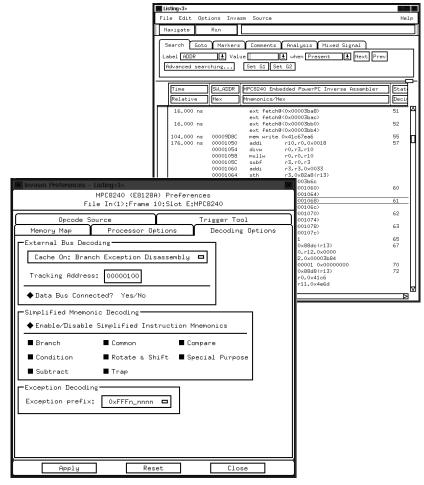


Figure 5: Inverse Assembler Options

## **PowerPC Cache-on Trace**

Modern embedded systems need tools to debug and characterize systems running at full performance. Agilent provides measurements that allow realtime trace and source correlation with the instruction cache enabled! This is a standard feature present in ALL PowerPC inverse assemblers for the 16700 logic analyzer family.

By using the PowerPC branch exception handler, the processor will write out change of flow markers to the external bus, which the logic analyzer will sample and reconstruct into the full program trace. Please refer to the emulation solution user manual for further implementation details. Refer to figure 5. Each section of assembly code is actually a single marker from the branch trace exception handler, reconstructed by the logic analyzer. In addition, cache-line fills are displayed as external memory accesses, allowing the user to differentiate between program flow and data traffic on the main memory bus. As always, Agilent's powerful filtering software allows you to select only certain types of information for viewing.

# **Modes of Operation**

## **State Modes**

In state-per-clock mode, address, data, and status are captured on each CPU clock. This mode is useful in hardware validation and analysis during system crashes.

In state-per-address or data-cycle modes for the MPC8260, the logic analyzer only records those states in which one or more of the strobes AACK, ARTRY, TA, DRTRY, or TEA are asserted. This mode filters wait states and exposes the PowerQUICC II microprocessor's decoupled address and data buses.

In state-per-address or data-cycle modes for the MPC8240, the logic analyzer only records those states in which the strobe MIV is asserted because there is no PPC 60X Bus visibility externally. This mode filters wait states and exposes the Motorola MPC8240 microprocessor's decoupled address and data buses.

# **Timing Mode**

Timing analysis is supported. All processor signals are connected directly to the logic analyzer pods.

# **Logic Analyzers Supported**

• Contact your Agilent field engineer for latest logic analyzer information.

## **PCI Measurements**

PCI support is available from: Future Plus Systems Corporation, 2790 N. Academy Blvd., Suite 307, Colorado Springs, CO 80917-5329. 719-380-7321

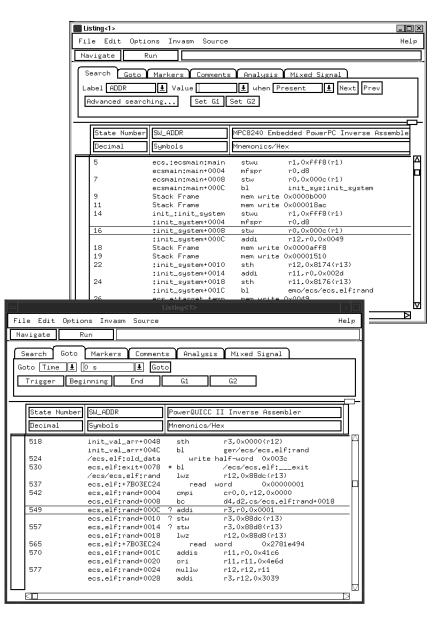


Figure 6: Inverse Assembler

## **Source Correlation Tool Set**

The inverse assembler can be used with the Agilent B4620B source correlation tool set for the 16700A Series logic analysis systems. This allows time correlation of an acquired trace to source code. The source correlation tool set uses the symbolic information provided in your object file to build a database of source files, line numbers and symbol information.

Once the logic analyzer acquires the real-time trace, you can step through the trace at assembly-code level or source-code level. You can also easily locate the cause of a problem by stepping backward to the root cause. With time-correlated analysis in both the digital and analog domains, Agilent provides powerful solutions for your most difficult hardware/software integration problems.

IEEE 695, Elf/Dwarf, Elf/Stabs, and ASCII symbol files are supported.

# **System Correlation**

With the logic analysis systems, you can time-correlate bus information from other microprocessors or bus interfaces in your target system, such as a PCI bus, with the Motorola MPC82XX. (Contact your local Test and Measurement sales office or visit our web site at http://www.agilent.com/find/las-data for more information).

# System Performance Analysis Tool Set\*

The system performance analysis (SPA) tool set is an optional software package for the Agilent 16700A Series logic analysis systems. The SPA tool set provides such statistical performance measurements as state overview, state interval, time interval, and time overview. The same symbol file used with the source correlation tool set provides symbolic support for the system performance analyzer, as shown in figure 8.

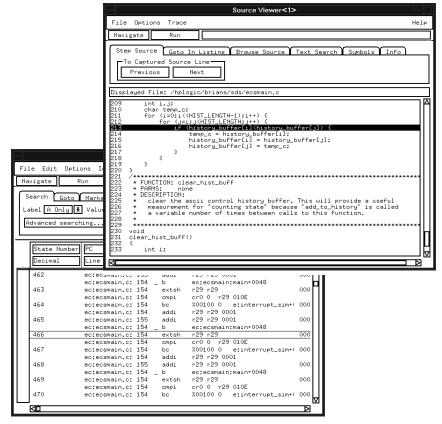


Figure 7: Inverse Assembled Trace Time-Correlated to Source Code Using the Source Correlation Tool Set

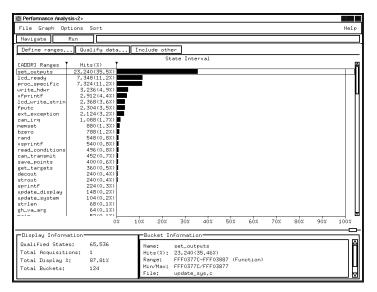


Figure 8: Statistical Performance Information from the System Performance Analysis Tool Set

<sup>\*</sup> The HP B4600B System Performance Analysis Tool Set is not available for MPC8240 but is available for MPC8260 in 60X bus mode.

# **Analysis Probes**

The analysis probes allows easy connection of a logic analyzer to your Motorola MPC8240 or MPC8260 BGA target system for real-time analysis. With the analysis probes, you don't need to design special debug connectors into your target system.

Mechanical dimensions are included in figure 10. The BGA sockets are soldered down in place of the microprocessors, as shown in figures 9 and 10. The microprocessors are inserted into BGA chip carrier sockets. The BGA chip carrier sockets can also be used directly with the BGA sockets on the target board without the analysis probes.

# "Keep Out" Area

The analysis probes require a minimal amount of "keep out" space around the

# The analysis probes consist of:

- Analysis probe board
- Inverse assembler and configuration files
- Two surface mount BGA sockets
- Soldering kit and instructions
- Three Agilent E5346A highdensity termination adapters
- Agilent E8161-60001 352-pin BGA probing kit (MPC8240 only)
   E8127-87607 extender
  - (MPC8240 only)
- Agilent E8160-60001 480-pin BGA probing kit (MPC8260 only)
   E8125-87607 extender
  - (MPC8260 only)

# Additional Accessories

- E8127-87607 extender (MPC8240 only)
- E8125-87607 extender (MPC8260 only)
- E5346A high-density termination adapter
- E8161-60001 BGA probing kit

microprocessor. The analysis probes also have an overhang, as shown on figures 21 and 23. The maximum height of components under the analysis probes in this area cannot exceed 15 mm or 0.591 inches. If components are too high for the clearance, order the Agilent E8125-87607 extender to add an additional 0.25 inches of clearance. Do not exceed two extenders with an analysis probe.

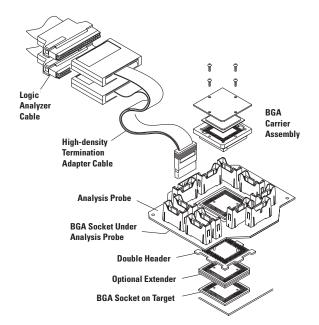


Figure 9: MPC8240 Analysis Probe

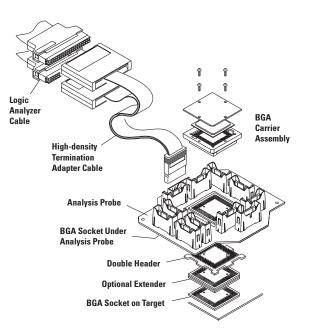


Figure 10: MPC8260 Analysis Probe

## Passively Probing the BGA Target System with Agilent Logic Analyzers

Signals required for inverse assembly are shown in the pinout information table beginning on page 18 and must be routed to AMP Mictor 38 connectors for the logic analyzer. Eight, 16-channel logic analyzer pods are required for inverse assembly. These eight pods are connected via the Mictor connectors to four highdensity termination adapters. The adapters are not included with the inverse assembler and must be ordered separately

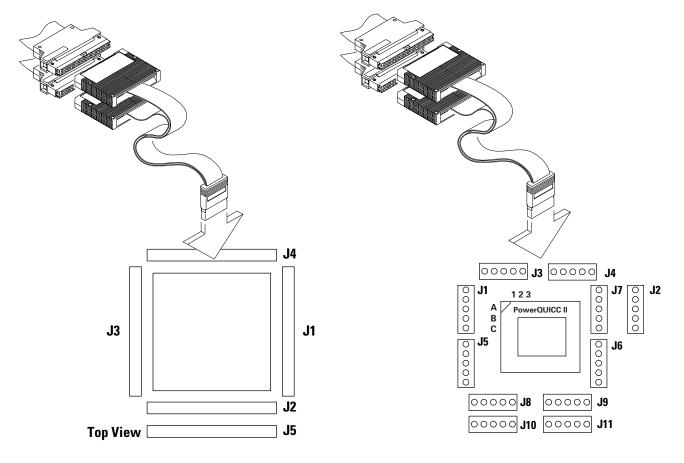


Figure 11. Connector Layout for a Motorola MPC8240 BGA Target

Figure 12. Connector Layout for a Motorola MPC8260 BGA Target

# Direct Connection through High-Density Adapter Cables

The Agilent E5346A high-density adapters use a minimal amount of board space. Each high-density adapter connects two logic analyzer pods, providing 32 channels of logic analysis per connector and access to two clock pins, as shown in figure 13.

Grounds need to be connected to pin 3 of the AMP Mictor connector. SCL, +5VDC and SDA are not to be connected electrically to the target system (pins 1, 2, and 4 on the Mictor connector).

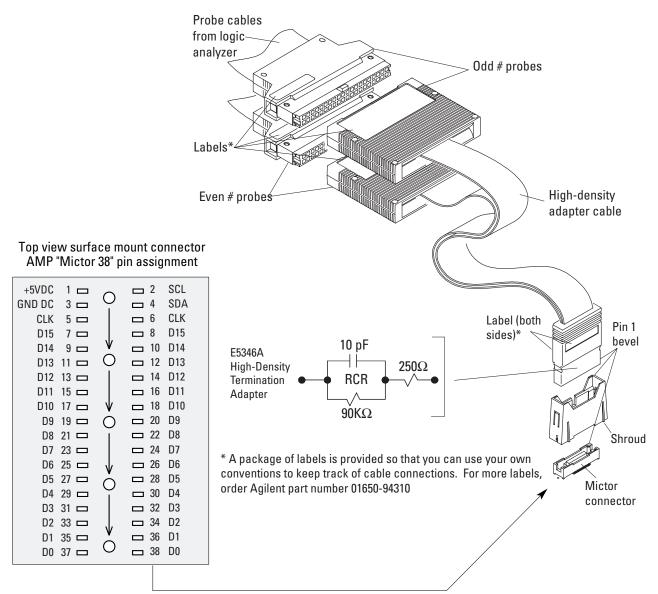


Figure 13. E5346A High-Density Termination Adapter

# **Signal Termination**

Termination for logic analysis is included at the probe tip of the E5346A high-density termination adapter for easy application and use. A schematic of this termination is shown in figure 14.

The AMP Mictor connector must be placed close enough to the target system so that the stub length created is less than 1/5 the Tr (bus risetime). For PC board material (er=4.9) and Zo in the range of  $50\text{-}80\Omega$ , use a propagation delay of 160 ps/inch of stub.

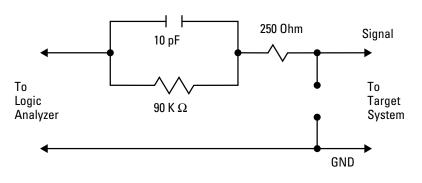


Figure 14. RC Network for Signal Termination

# **Mictor Connector Placement**

Four E5346A adapters and Mictor connectors are needed to probe all the required signals for inverse assembly.

Placing the AMP Mictor connectors as close as possible to the signal source will minimize stub length and ensure a reliable measurement. Figures 15 and 16 shows the connector layout of J1-J5. J1-J4 are required for inverse assembly. J5 is optional for timing or state analysis of I/O ports.

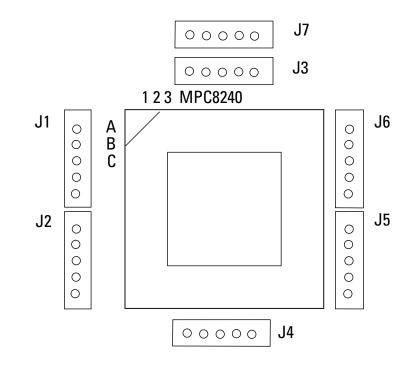


Figure 15. Mictor Connector Placement for the MPC8240

**Mictor Connector** 

The AMP Mictor connectors are available from AMP (PN 2-767004-2) or from Agilent Technologies (PN E5346-68701). The Agilent Mictor kit contains five AMP Mictor connectors and five support shrouds. The signals +5 VDC, SCL, and SDA are not used for probing and should not be connected electrically to the target system, as shown in figure 13.

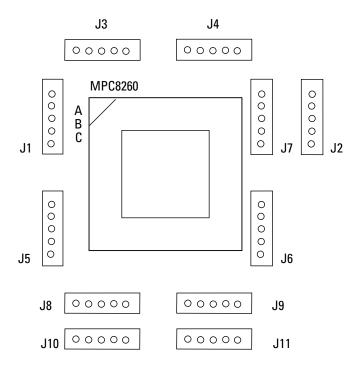


Figure 16. Mictor Connector Placement for the MPC8260

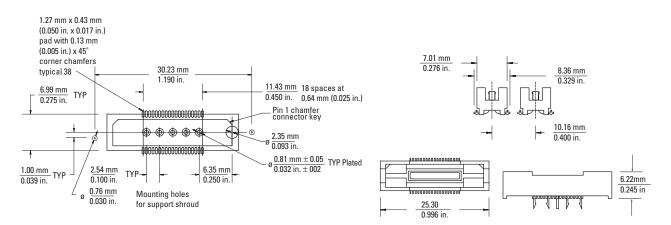


Figure 17. AMP Mictor Connector Dimensions

## **Support Shroud**

A support shroud (Agilent E5346-44701) is recommended to provide additional strain relief between the E5346A adapter and the AMP Mictor connector, as shown in figure 18. The shroud fits around the AMP Mictor connector and requires two through-hole connections to the target board. Five shrouds are included with five AMP Mictor connectors in the E5346-68701 kit.

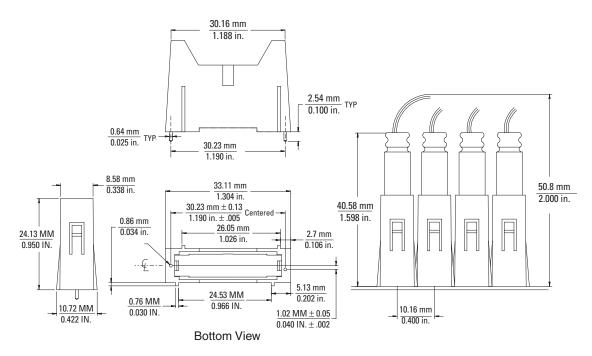


Figure 18. Support Shroud Dimensions

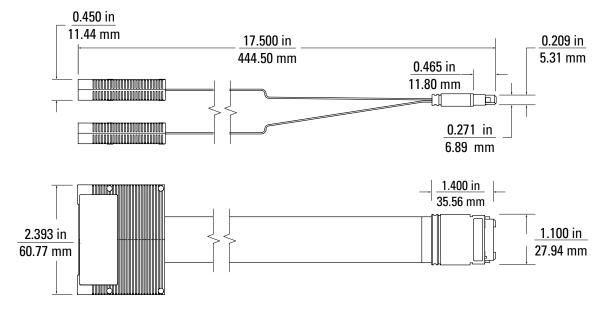


Figure 19. High-Density Termination Adapter Cable Dimensions

# MPC8240 Pinout Information on Required Signals for Inverse Assembly

This table describes the connections for the four Mictor 38 connectors necessary for compatibility with the inverse assembler and the E5346A high-density termination adapter cables. This is intended to be a guide for placing probing connectors on a target system.

J1-J4 are required for full inverse assembly and if no data visibility is required, J1-J2 need to be connected for code-flow only.

Mictor Conn. #	AMP Mictor Pin#	Signal Name	Mictor Conn. #	AMP Mictor Pin #	Signal Name
J1 (odd)	38	SDMA[0]	J1 [even]	37	Debug_Addr[2] /FTP[3]
	36	SDMA[1]		35	Debug_Addr[3] /PCI_CLK[4]
	34	SDMA[2]		33	Debug_Addr[4] /REQ[4]
	32	SDMA[3]		31	Debug_Addr[5] /GNT[4]
	30	SDMA[4]		29	Debug_Addr[6] /PLL_CFG[4]
	28	SDMA[5]		27	Debug_Addr[7] /PLL_CFG[3]
	26	SDMA[6]		25	Debug_Addr[8] /PLL_CFG[2]
	24	SDMA[7]		23	Debug_Addr[9] /PLL_CFG[1]
	22	SDMA[8]		21	Debug_Addr[10] /PLL_CFG[0]
	20	SDMA[9]		19	Debug_Addr[11] /FTP[2]
	18	SDMA[10]		17	Debug_Addr[12] /FTP[1]
	16	SDMA[11]		15	Debug_Addr[13] /FTP[0]
	14	SDMA0[12]/SDBA1		13	Debug_Addr[14] /MTP[1]
	12	SDBA0		11	Debug_Addr[15] /MTP[0]
	10	Debug_Addr[0]/#QACK		9	CKE
	8	Debug_Addr[1]/CKO		7	RTC
	6	SDRAM_CLK[0]		5	#MIV

Mictor	AMP Mictor	Signal Name	Mictor	AMP Mictor	Signal Name
Conn. #	Pin#		Conn. #	Pin #	
J2 (odd)	38	MAA[2]	J2 (even)	37	CAS/#DQM[7]
	36	MAA[1]		35	CAS/#DQM[6]
	34	MAA[0]		33	CAS/#DQM[5]
	32	#RCS1		31	CAS/#DQM[4]
	30	#RCS0		29	CAS/#DQM[3]
	28	RAS/#CS[7]		27	CAS/#DQM[2]
	26	RAS/#CS[6]		25	CAS/#DQM[1]
	24	RAS/#CS[5]		23	CAS/#DQM[0]
	22	RAS/#CS[4]		21	PAR/AR[7]
	20	RAS/#CS[3]		19	PAR/AR[6]
	18	RAS/#CS[2]		17	PAR/AR[5]
	16	RAS/#CS[1]		15	PAR/AR[4]
	14	RAS/#CS[0]		13	PAR/AR[3]
	12	#AS		11	PAR/AR[2]
	10	#WE		9	PAR/AR[1]
	8	#FOE		7	PAR/AR[0]
	6	#SDRAS		5	#SDCAS
Mictor	AMP Mictor	Signal Name	Mictor	AMP Mictor	Signal Name
Conn. #	Pin#		Conn. #	Pin #	
J3 (odd)	38	DH[31]	J3 (even)	37	DL[31](LSB)
	36	DH[30]		35	DL[30]
	34	DH[29]		33	DL[29]
	32	DH[28]		31	DL[28]
	30	DH[27]		29	DL[27]
	28	DH[26]		27	DL[26]
	26	DH[25]		25	DL[25]
	24	DH[24]		23	DL[24]
	22	DH[23]		21	DL[23]
	20	DH[22]		19	DL[22]
	18	DH[21]		17	DL[21]
	16	DH[20]		15	DL[20]
	14	DH[19]		13	DL[19]
	12	DH[18]		11	DL[18]
				•	DI [47]
	10	DH[17]		9	DL[17]
	10 8	DH[17] DH[16]		9 7	DL[17] DL[16]

Mictor Conn. #	AMP Mictor Pin#	Signal Name	Mictor Conn. #	AMP Mictor Pin #	Signal Name
J4 (odd)	38	DH[15]	J4 (even)	37	DL[15]
	36	DH[14]		35	DL[14]
	34	DH[13]		33	DL[13]
	32	DH[12]		31	DL[12]
	30	DH[11]		29	DL[11]
	28	DH[10]		27	DL[10]
	26	DH[9]		25	DL[9]
	24	DH[8]		23	DL[8]
	22	DH[7]		21	DL[7]
	20	DH[6]		19	DL[6]
	18	DH[5]		17	DL[5]
	16	DH[4]		15	DL[4]
	14	DH[3		13	DL[3]
	12	DH[2		11	DL[2
	10	DH[1]		9	DL[1]
	8	DH[0] (MSB)		7	DL[0]
	6			5	
Mictor	AMP Mictor	Signal Name	Mictor	AMP Mictor	Signal Name
Mictor Conn. #	AMP Mictor Pin#	Signal Name	Mictor Conn. #	AMP Mictor Pin #	Signal Name
Conn. #	Pin#		Conn. #	Pin #	Signal Name
	<b>Pin#</b>	PAR		<b>Pin #</b> 37	Signal Name
Conn. #	<b>Pin#</b> 38 36	PAR #SERR	Conn. #	<b>Pin #</b> 37 35	
Conn. #	Pin# 38 36 34	PAR #SERR #PERR	Conn. #	Pin # 37 35 33	IDSEL
Conn. #	Pin# 38 36 34 32	PAR #SERR #PERR #LOCK	Conn. #	Pin # 37 35 33 31	IDSEL #GNT[0]
Conn. #	Pin# 38 36 34 32 30	PAR #SERR #PERR #LOCK #STOP	Conn. #	Pin # 37 35 33 31 29	IDSEL
Conn. #	Pin# 38 36 34 32 30 28	PAR #SERR #PERR #LOCK #STOP #DEVSEL	Conn. #	Pin # 37 35 33 31 29 27	IDSEL #GNT[0] #REQ[0]
Conn. #	Pin# 38 36 34 32 30 28 26	PAR #SERR #PERR #LOCK #STOP #DEVSEL C/#BE[0]	Conn. #	Pin # 37 35 33 31 29 27 25	IDSEL #GNT[0] #REQ[0] GND
Conn. #	Pin# 38 36 34 32 30 28 26 24	PAR #SERR #PERR #LOCK #STOP #DEVSEL C/#BE[0] C/#BE[1]	Conn. #	Pin # 37 35 33 31 29 27 25 23	IDSEL #GNT[0] #REQ[0] GND #IRDY
Conn. #	Pin# 38 36 34 32 30 28 26 24 22	PAR #SERR #PERR #LOCK #STOP #DEVSEL C/#BE[0] C/#BE[1] C/#BE[2]	Conn. #	Pin # 37 35 33 31 29 27 25 23 21	IDSEL #GNT[0] #REQ[0] GND #IRDY #FRAME
Conn. #	Pin# 38 36 34 32 30 28 26 24 22 20	PAR #SERR #PERR #LOCK #STOP #DEVSEL C/#BE[0] C/#BE[1]	Conn. #	Pin # 37 35 33 31 29 27 25 23 21 19	IDSEL #GNT[0] #REQ[0] GND #IRDY #FRAME #TRDY
Conn. #	Pin# 38 36 34 32 30 28 26 24 22 20 18	PAR #SERR #PERR #LOCK #STOP #DEVSEL C/#BE[0] C/#BE[1] C/#BE[2] C/#BE[3]	Conn. #	Pin # 37 35 33 31 29 27 25 23 21 19 17	IDSEL #GNT[0] #REQ[0] GND #IRDY #FRAME #TRDY #GNT[1]
Conn. #	Pin# 38 36 34 32 30 28 26 24 22 20 18 16	PAR #SERR #PERR #LOCK #STOP #DEVSEL C/#BE[0] C/#BE[1] C/#BE[2]	Conn. #	Pin # 37 35 33 31 29 27 25 23 21 19 17 15	IDSEL #GNT[0] #REQ[0] GND #IRDY #FRAME #TRDY #GNT[1] #REQ[1]
Conn. #	Pin#           38           36           34           32           30           28           26           24           22           20           18           16           14	PAR #SERR #PERR #LOCK #STOP #DEVSEL C/#BE[0] C/#BE[1] C/#BE[2] C/#BE[3]	Conn. #	Pin # 37 35 33 31 29 27 25 23 21 19 17 15 13	IDSEL #GNT[0] #REQ[0] GND #IRDY #FRAME #TRDY #GNT[1] #REQ[1] PMAA[2]
Conn. #	Pin#           38           36           34           32           30           28           26           24           22           20           18           16           14           12	PAR #SERR #PERR #LOCK #STOP #DEVSEL C/#BE[0] C/#BE[1] C/#BE[2] C/#BE[3]	Conn. #	Pin # 37 35 33 31 29 27 25 23 21 19 17 15 13 11	IDSEL #GNT[0] #REQ[0] GND #IRDY #FRAME #TRDY #GNT[1] #REQ[1] PMAA[2] PMAA[1]
Conn. #	Pin#           38           36           34           32           30           28           26           24           22           20           18           16           14           12           10	PAR #SERR #PERR #LOCK #STOP #DEVSEL C/#BE[0] C/#BE[1] C/#BE[2] C/#BE[3]	Conn. #	Pin # 37 35 33 31 29 27 25 23 21 19 17 15 13 11 9	IDSEL #GNT[0] #REQ[0] GND #IRDY #FRAME #TRDY #GNT[1] #REQ[1] PMAA[2]
Conn. #	Pin#           38           36           34           32           30           28           26           24           22           20           18           16           14           12	PAR #SERR #PERR #LOCK #STOP #DEVSEL C/#BE[0] C/#BE[1] C/#BE[2] C/#BE[3]	Conn. #	Pin # 37 35 33 31 29 27 25 23 21 19 17 15 13 11	IDSEL #GNT[0] #REQ[0] GND #IRDY #FRAME #TRDY #GNT[1] #REQ[1] PMAA[2] PMAA[1]

Mictor Conn. #	AMP Mictor Pin#	Signal Name	Mictor Conn. #	AMP Mictor Pin #	Signal Name
J6 (odd)	38	AD[0](LSB)	J6 (even)	37	AD[16]
	36	AD[1]		35	AD[17]
	34	AD[2]		33	AD[18]
	32	AD[3]		31	AD[19]
	30	AD[4]		29	AD[20]
	28	AD[5]		27	AD[21]
	26	AD[6]		25	AD[22]
	24	AD[7]		23	AD[23]
	22	AD[8]		21	AD[24]
	20	AD[9]		19	AD[25]
	18	AD[10]		17	AD[26]
	16	AD[11]		15	AD[27]
	14	AD[12]		13	AD[28]
	12	AD[13		11	AD[29]
	10	AD[14]		9	AD[30]
	8	AD[15]		7	AD[31] (MSB)
	6			5	
Mictor	AMP Mictor	Signal Name	Mictor	AMP Mictor	Signal Name
					orginar manne
Conn. #	Pin#		Conn. #	Pin #	
	Pin#		Conn. #	Pin #	
<b>Conn. #</b> J7 (odd)	<b>Pin#</b>	CHKSTOP_IN		<b>Pin #</b>	#SMI
	<b>Pin#</b> 38 36	CHKSTOP_IN SCL	Conn. #	<b>Pin #</b> 37 35	#SMI NMI
	Pin# 38 36 34	CHKSTOP_IN SCL SDA	Conn. #	Pin # 37 35 33	#SMI NMI #MCP
	Pin# 38 36 34 32	CHKSTOP_IN SCL SDA IRQ4/LINT	Conn. #	Pin # 37 35 33 31	#SMI NMI #MCP #HRST_CPU
	Pin# 38 36 34 32 30	CHKSTOP_IN SCL SDA IRQ4/LINT IRQ3/#S_FRAME	Conn. #	Pin # 37 35 33 31 29	#SMI NMI #MCP
	Pin# 38 36 34 32 30 28	CHKSTOP_IN SCL SDA IRQ4/LINT IRQ3/#S_FRAME IRQ2/S_RST	Conn. #	Pin # 37 35 33 31 29 27	#SMI NMI #MCP #HRST_CPU
	Pin# 38 36 34 32 30 28 26	CHKSTOP_IN SCL SDA IRQ4/LINT IRQ3/#S_FRAME IRQ2/S_RST IRQ1/S_CLK	Conn. #	Pin # 37 35 33 31 29 27 25	#SMI NMI #MCP #HRST_CPU
	Pin# 38 36 34 32 30 28 26 24	CHKSTOP_IN SCL SDA IRQ4/LINT IRQ3/#S_FRAME IRQ2/S_RST IRQ1/S_CLK IRQ0/S_INT	Conn. #	Pin # 37 35 33 31 29 27 25 23	#SMI NMI #MCP #HRST_CPU
	Pin# 38 36 34 32 30 28 26 24 22	CHKSTOP_IN SCL SDA IRQ4/LINT IRQ3/#S_FRAME IRQ2/S_RST IRQ1/S_CLK IRQ0/S_INT #TRST	Conn. #	Pin # 37 35 33 31 29 27 25 23 21	#SMI NMI #MCP #HRST_CPU
	Pin# 38 36 34 32 30 28 26 24 22 20	CHKSTOP_IN SCL SDA IRQ4/LINT IRQ3/#S_FRAME IRQ2/S_RST IRQ1/S_CLK IRQ0/S_INT #TRST TMS	Conn. #	Pin # 37 35 33 31 29 27 25 23 23 21 19	#SMI NMI #MCP #HRST_CPU
	Pin# 38 36 34 32 30 28 26 24 22 20 18	CHKSTOP_IN SCL SDA IRQ4/LINT IRQ3/#S_FRAME IRQ2/S_RST IRQ1/S_CLK IRQ0/S_INT #TRST TMS TDO	Conn. #	Pin # 37 35 33 31 29 27 25 23 21 19 17	#SMI NMI #MCP #HRST_CPU
	Pin# 38 36 34 32 30 28 26 24 22 20 18 16	CHKSTOP_IN SCL SDA IRQ4/LINT IRQ3/#S_FRAME IRQ2/S_RST IRQ1/S_CLK IRQ0/S_INT #TRST TMS TD0 TDI	Conn. #	Pin # 37 35 33 31 29 27 25 23 21 19 17 15	#SMI NMI #MCP #HRST_CPU
	Pin# 38 36 34 32 30 28 26 24 22 20 18 16 14	CHKSTOP_IN SCL SDA IRQ4/LINT IRQ3/#S_FRAME IRQ2/S_RST IRQ1/S_CLK IRQ0/S_INT #TRST TMS TDO TDI TCK	Conn. #	Pin # 37 35 33 31 29 27 25 23 21 19 17 15 13	#SMI NMI #MCP #HRST_CPU
	Pin# 38 36 34 32 30 28 26 24 22 20 18 16 14 12	CHKSTOP_IN SCL SDA IRQ4/LINT IRQ3/#S_FRAME IRQ2/S_RST IRQ1/S_CLK IRQ0/S_INT #TRST TMS TDO TDI TCK TBEN	Conn. #	Pin # 37 35 33 31 29 27 25 23 21 19 17 15 13 11	#SMI NMI #MCP #HRST_CPU
	Pin# 38 36 34 32 30 28 26 24 22 20 18 16 14	CHKSTOP_IN SCL SDA IRQ4/LINT IRQ3/#S_FRAME IRQ2/S_RST IRQ1/S_CLK IRQ0/S_INT #TRST TMS TDO TDI TCK	Conn. #	Pin # 37 35 33 31 29 27 25 23 21 19 17 15 13	#SMI NMI #MCP #HRST_CPU

# Recommended Pinout Information for MPC8260 Inverse Assembly

The following tables describe the recommended pinout for full PowerQUICC II analysis. The pinouts are compatible with the inverse assembler and the E5346A high-density termination adapter cables. They are intended to be a guide for placing probing connectors on the target system.

J1-J5 are required for inverse assembly. J6-J7 are required for PCI/localbus analysis. The remaining connectors are optional.

The recommended pinout is designed for minimal trace lengths. The tradeoff is that a 5th connector/cable is required for inverse assembly. Note that the IA still only requires 8-pods for inverse assembly. The next section has an alternative pinout, which requires only four connectors for inverse assembly

Mictor Conn. #	AMP Mictor Pin#	Signal Name	Mictor Conn. #	AMP Mictor Pin #	Signal Name
J1 (odd)	38	BADDR31 (LSB)	J1 (even)	37	A15
	36	BADDR30	. (,	35	A14
	34	BADDR29		33	A13
	32	BADDR28		31	A12
	30	BADDR27		29	A11
	28	A26		27	A10
	26	A25		25	A9
	24	A24		23	A8
	22	A23		21	A7
	20	A22		19	A6
	18	A21		17	A5
	16	A20		15	A4
	14	A19		13	A3
	12	A18		11	A2
	10	A17		9	A1
	8	A16		7	A0
	6	CLKIN		5	#DVAL
12 (add)	20	Reserved	12 (avan)	27	#CS11
J2 (odd)	38 36	Reserved	J2 (even)	37 35	#CS10
	30 34	Reserved		33	#CS9
	34 32	DP7/CSE1		33 31	#CS9 #CS8
	32 30	DP6/CSE0		29	#CS8 #CS7
	28			29 27	#CS6
		DP5 DP4		25	#CS6 #CS5
	26 24	DP4 DP3		23	#CS5 #CS4
	24 22	DP3 DP2		23	#034 #PWE7
	20	DP1		19	#PWE6
	18	DP0		17	#PWE5
	16	#BCTL0		15	#PWE4
	14	PSDAMUX		13	#PWE3
	12	#PGTA		11	#PWE2
	10	PSDA10		9	#PWE1
	8	#PSDWE		7	#PWE0
	6	Reserved		5	#PSDCAS

Although Motorola connects pin 3 to ground for the ADS board, we do not recommend connecting it.

Mictor Conn. #	AMP Mictor Pin#	Signal Name	Mictor Conn. #	AMP Mictor Pin #	Signal Name
J3 (odd)	38	D63(LSB)	J3 (even)	37	D47
	36	D62		35	D46
	34	D61		33	D45
	32	D60		31	D44
	30	D59		29	D43
	28	D58		27	D42
	26	D57		25	D41
	24	D56		23	D40
	22	D55		21	D39
	20	D54		19	D38
	18	D53		17	D37
	16	D52		15	D36
	14	D52		13	D35
	12	D50		11	D34
	10	D49		9	D33
	8	D48		7	D32
	6	#CS3		5	#CS2
	0	#000		5	#002
J4 (odd)	38	D31	J4 (even)	37	D15
	36	D30		35	D14
	34	D29		33	D13
	32	D28		31	D12
	30	D27		29	D11
	28	D26		27	D10
	26	D25		25	D9
	24	D24		23	D8
	22	D23		21	D7
	20	D22		19	D6
	18	D21		17	D5
	16	D20		15	D4
	14	D19		13	D3
	12	D18		11	D3 D2
	10	D10		9	D1
	8	D16		7	D0(MSB)
	6	#CS1		5	#CS0
J5 (odd)	38	TC1	J5 (even)	37	#PORST
	36	TC0		35	#SRESET
	34	#TEA		33	#HRESET
	32	#TA		31	#CPU_BR
	30	TT4		29	#L2
	28	TT3		27	GBL
	26	TT2		25	TC2
	24	TT1		23	#DBB
	22	ТТО		21	#DBG
	20	TSIZ3		19	ALE
	18	TSIZ2		17	#BR
	16	TSIZ1		15	#CPU_DBG
	14	TSIZO		13	#NMI_OUT
	14	#PSDRAS/#POE		13	#INIVII_001 #BG
	12				
		#ARTRY		9 7	#ABB #APE
	8 6	#TBST #AACK		7 5	#APE #TS

Mictor	AMP Mictor	Signal Name	Mictor	AMP Mictor	Signal Name
Conn. #	Pin#		Conn. #	Pin #	4.0.10
J6 (odd)	38	AD0 (LSB)	J6 (even)	37	AD16
	36	AD1		35	AD17
	34	AD2		33	AD18
	32	AD3		31	AD19
	30	AD4		29	AD20
	28	AD5		27	AD21
	26	AD5		25	AD22
	24	AD7		23	AD23
	22	AD8		21	AD24
	20	AD9		19	AD25
	18	AD10		17	AD26
	16	AD11		15	AD27
	14	AD12		13	AD28
	12	AD13		11	AD29
	10	AD14		9	AD30
	8	AD15		7	AD31(MSB)
	6	PCI_CLK		5	#LSDCAS
Mictor Conn. #	AMP Mictor Pin#	Signal Name	Mictor Conn. #	AMP Mictor Pin #	Signal Name
J7 (odd)	38	L_A31	J7 (even)	37	L_A15/#FRAME
	36	L_A30/#LOCK		35	L_A14/#PAR
	34	L_A29/#INTA		33	L_DP3
	32	L_A2/8#RST		31	L_DP2
	30	L_A27		29	L_DP1
	28			27	L_DP0
	26	L_A25/#GNT0		25	#LBS3
	24	L_A24		23	#LBS2
	22	L_A23/#REQ0		21	#LBS1
	20	L_A22/#SERR		19	#LBS0
	18	L_A21/#PERR		17	#LSDRAS/#LOE
	16	L_A20/#IDSEL		15	#LWR
	14	L_A19/#DEVSEL		13	LSDA10
	12	L_A18/#STOP		11	#LSDAWE
	10	L_A17/#IRDY		9	LSDAMUX
	8			J 7	LODAMOX
	о 6	L_A16/#TRDY CLKIN		5	#LGTA
	0	GLNIN		5	#LUTA
J8 (odd)	38	PA31	J8 (even)	37	PA15
00 (0uu)	36	PA30	00 (even)	35	PA15 PA14
		PA30 PA29			
	34 32	PA29 PA28		33 31	PA13 PA12
	32 30	PA28 PA27		29	PA12 PA11
				29 27	PATT PATO
	28 26	PA26 PA25		27 25	PATU PA9
	26 24				PA9 PA8
		PA24		23	
	22	PA23		21	PA7
	20	PA22		19	PA6
	20	DA01		17	PA5
	18	PA21		45	
	18 16	PA20		15	PA4
	18 16 14	PA20 PA19		13	PA3
	18 16 14 12	PA20 PA19 PA18		13 11	PA3 PA2
	18 16 14 12 10	PA20 PA19 PA18 PA17		13 11 9	PA3 PA2 PA1
	18 16 14 12	PA20 PA19 PA18		13 11	PA3 PA2

Mictor Conn. #	AMP Mictor Pin#	Signal Name	Mictor Conn. #	AMP Mictor Pin #	Signal Name
J9 (odd)	38	PB31	J9 (even)	37	PB15
00 (000)	36	PB30	00 (67611)	35	PB14
	34	PB29		33	PB14 PB13
	34 32	PB28		33 31	PB12
	30	PB27		29	PB11
	28	PB26		27	PB10
	26	PB25		25	PB9
	24	PB24		23	PB8
	22	PB23		21	PB7
	20	PB22		19	PB6
	18	PB21		17	PB5
	16	PB20		15	PB4
	14	PB19		13	
	12	PB18		11	
	10	PB17		9	
	8	PB16		7	
	6	NC		5	NC
	0			5	NO
J10 (odd)	38	PC31	J10 (even)		PC15
	36	PC30		35	PC14
	34	PC29		33	PC13
	32	PC28		31	PC12
	30	PC27		29	PC11
	28	PC26		27	PC10
	26	PC25		25	PC9
	24	PC24		23	PC8
	24	PC23		21	PC7
	20	PC22		19	PC6
	18	PC21		17	PC5
	16	PC20		15	PC4
	14	PC19		13	PC3
	12	PC18		11	PC2
	10	PC17		9	PC1
	8	PC16		7	PC0
	6	NC		5	NC
J11 (odd)	38	PD31	J11 (even)	37	PD15
	36	PD30	011 (67611)	35	PD14
	30 34			33	PD14 PD13
		PD29			PD13 PD12
	32	PD28		31 20	
	30	PD27		29	PD11
	28	PD26		27	PD10
	26	PD25		25	PD9
	24	PD24		23	PD8
	22	PD23		21	PD7
	20	PD22		19	PD6
	18	PD21		17	PD5
	16	PD20		15	PD4
	14	PD19		13	
	12	PD18		11	
	10	PD17		9	
	8	PD16		3 7	
	6	NC		5	NC
	0			0	

# Alternative MPC8260 Pinout Information for Inverse Assembly

The following tables describe the alternative pinout for full PowerQUICC II analysis. The pinouts are compatible with the inverse assembler and the E5346A high-density termination adapter cables. This is intended to be a guide for placing probing connectors on the target system.

J1-J4 are required for inverse assembly. J6-J7 are required for PCI/local-bus analysis. The remaining connectors are optional.

The alternative pinout is included for those interested in inverse assembly only. This pinout requires only four connectors. However, signals must be routed across the chip resulting in longer trace lengths. The recommended pinout in the previous section is the electrically superior configuration.

Mictor Conn. #	AMP Mictor Pin#	Signal Name	Mictor Conn. #	AMP Mictor Pin #	Signal Name
J1 (odd)	38	BADDR31 (LSB)	J1 (even)	37	A15
,	36	BADDR30	- ( )	35	A14
	34	BADDR29		33	A13
	.32	BADDR28		31	A12
	30	BADDR27		29	A11
	28	A26		27	A10
	26	A25		25	A9
	24	A24		23	A8
	22	A23		21	A7
	20	A22		19	A6
	18	A21		17	A5
	16	A20		15	A4
	14	A19		13	A3
	12	A18		11	A2
	10	A17		9	A1
	8	A16		7	A0
	6	CLKIN		5	#DVAL
J2 (odd)	38	TC1	J2 (even)	37	#CS11
02 (000)	36	TCO	02 (010)	35	#CS10
	34	#TEA		33	#CS9
	32	#TA		31	#CS8
	30	TT4		29	#CS7
	28	TT3		27	#CS6
	26	TT2		25	#CS5
	24	TT1		23	#CS4
	22	TT0		21	#PWE7
	20	TSIZ3		19	#PWE6
	18	TSIZ2		17	#PWE5
	16	TSIZ1		15	#PWE4
	14	TSIZO		13	#PWE3
	12	#PSDRAS/#POE		11	#PWE2
	10	#ARTRY		9	#PWE1
	8	#TBST		7	#PWE0
	6	#AACK		5	#PSDCAS

Mictor	AMP Mictor	Signal Name	Mictor	AMP Mictor	Signal Name
Conn. #	Pin#	Dac/( 0D)	Conn. #	Pin #	5.5
J3 (odd)	38	D63(LSB)	J3 (even)	37	D47
	36	D62		35	D46
	34	D61		33	D45
	32	D60		31	D44
	30	D59		29	D43
	28	D58		27	D42
	26	D57		25	D41
	24	D56		23	D40
	22	D55		21	D39
	20	D54		19	D38
	18	D53		17	D37
	16	D52		15	D36
	14	D52		13	D35
	12	D50		11	D34
	10	D49		9	D33
	8	D48		7	D32
	6	#CS3		5	#CS2
J4 (odd)	38	D31	J4 (even)	37	D15
04 (Uuu)			J4 (even)		
	36	D30		35	D14
	34	D29		33	D13
	32	D28		31	D12
	30	D27		29	D11
	28	D26		27	D10
	26	D25		25	D9
	24	D24		23	D8
	22	D23		21	D7
	20	D22		19	D6
	18	D21		17	D5
	16	D20		15	D4
	14	D19		13	D3
	12	D18		10	D2
	10	D17		9	D1
	8	D16		7	D0(MSB)
	6	#CS1		5	#CS0
J5 (odd)	38	RESERVED	J5 (even)	37	#[PRST
00 (000)	36	RESERVED	00 (01011)	35	#SRESET
	34			33	#HRESET
		RESERVED			
	32	DP7/CSE1		31	#CPU_BR
	30	DP6/CSE0		29	#L2_HIT
	28	DP5		27	GBL
	26	DP4		25	TC2
	24	DP3		23	#DBB
	22	DP2		21	#DBG
	20	DP1		19	ALE
	18	DP0		17	#BR
	16	#BCTL0		15	#CPU_DBG
	14	PSDAMUX		13	#NMI_OUT
	14	#PGTA		11	#BG
	12	#PSDA10		9	#ABB
	8	#PSDWE		7	#APE
	6	RESERVED		5	#TS

Note: J6-J11 are the same as the recommended pinout

#### **Analysis Probes Mechanical Information**

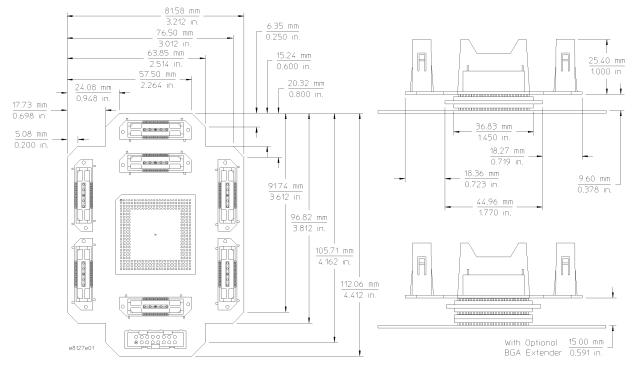


Figure 20: MPC8240 Analysis Probe Dimensions

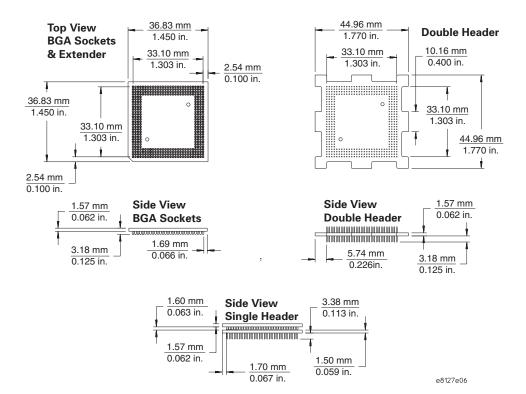


Figure 21: MPC8240 BGA Socket and Keep-Out Area

# **Analysis Probes Mechanical Information**

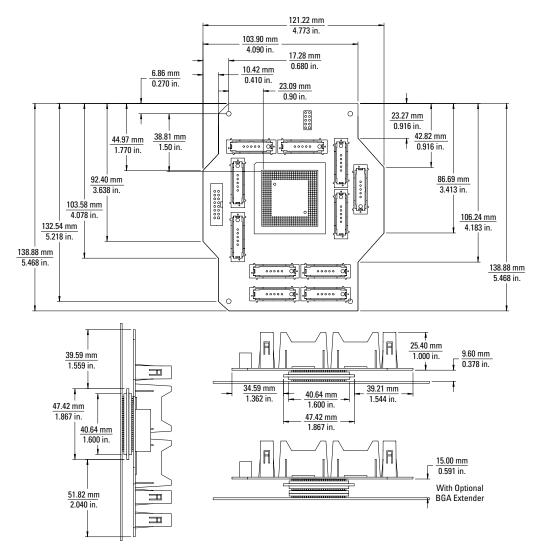


Figure 20: MPC8240 Analysis Probe Dimensions

# **Analysis Probes Mechanical Information**

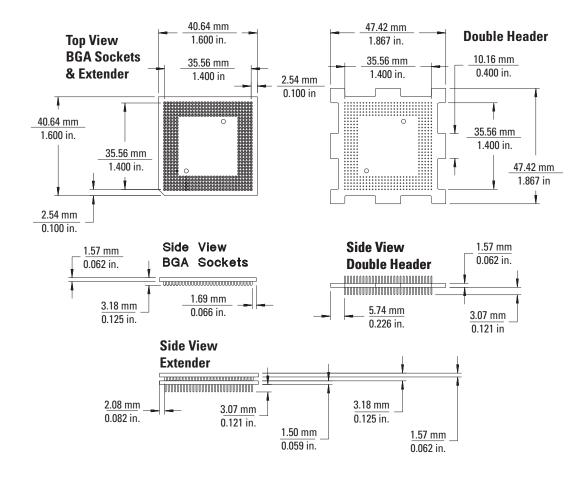
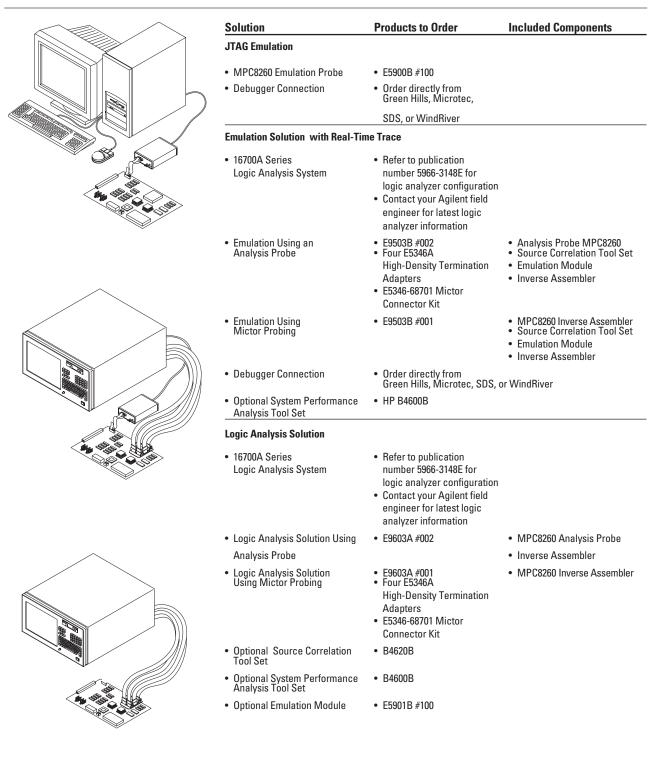


Figure 21: MPC8240 BGA Socket and Keep-Out Area

# Motorola MPC8260 System Configuration and Ordering Information

The table below shows the system components you need to order and what is included in each. The solution product numbers do not include logic analysis. The 16700A Series logic analysis systems must be ordered separately.

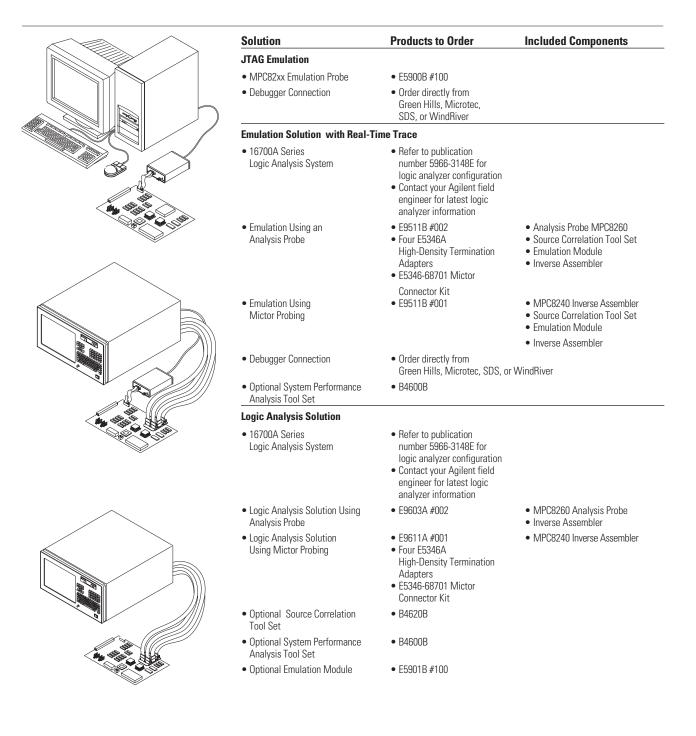
If you want to configure or upgrade your system with individual products, see page 33 for individual product number information.



## Motorola MPC8240 System Configuration and Ordering Information

The table below shows the system components you need to order and what is included in each. The solution product numbers do not include logic analysis. The 16700A Series logic analysis systems must be ordered separately.

If you want to configure or upgrade your system with individual products, see page 33 for individual product number information.



#### **Individual Components Ordering Information**

Description	Agilent Product
Emulation Probe	E5900B #100
Emulation Module	E5901B #100
MPC8260 Inverse Assembler	E9603A #001
MPC8240 Inverse Assembler	E9611A #001
Emulation Probe Migration	E5902B #100
Source Correlation Tool Set	B4620B
System Performance Analysis Tool Set	B4600B
High-Density Termination Adapter	E5346A
Mictor Connector Kit	E5346-68701
MPC8260 BGA Probing Kit with two sockets	E8160-60001
MPC8240 BGA Probing Kit with two sockets	E8161-60001
High-Density Right Angle Adapter	E5346-63201
High-Density Termination Adapter Support Shroud	E5346-44701
AMP Mictor Connector (order from AMP)	AMP PN 2-767004-2
High-Density Right Angle Adapter	E5346-63201
High-Density Termination Adapter Support Shroud	E5346-44701

Related Literature	Pub. Number
HP 16600A and 16700A Series Logic Analysis System Mainframes, Product Overview	5966-3107E
Probing Solutions for HP Logic Analysis Systems	5968-4632E
Processor and Bus Support for Agilent Technologies Logic Analyzers, Configuration Guide	5966-4365E

#### **Training and Consulting**

Agilent Technologies has experienced Digital Systems Consultants who can help you maximize the use of your emulation and analysis system through training and consulting. Digital Systems Consultants are experienced in debugging complex digital hardware/software problems and hardware/software integration.

Training can be delivered through scheduled courses, on-site classes, or one-on-one consulting. Agilent Technologies has courses for the beginner as well as advanced users migrating from the Agilent 16500 Series systems. Call 1-800-593-6632 in the U.S. for information about training schedules and location or to register. For training offered in other countries and languages, consult the Test and Measurement education web site: http://www.hp.com/go/tmeducation.

For consulting services, contact your local Test and Measurement sales office. A digital systems consultant can help you solve tough digital debug problems by showing you how to apply Agilent Technologies tools and debug best practices. Topics covered can include:

- System Installation
- Complex Triggering
- Multiple Bus Analysis
- Source-Line Referencing
- System Performance Analysis
- Instrumenting Code to Solve Specific Issues
- Bus Signal Timing Analysis
- Signal Integrity Analysis
- 16700A/1660XA Networking

Topics related to debug of Motorola MPC82XX microprocessor-based targets can include:

- Instruction/Data Cache Issues
- Checkstop Analysis
- Single and Multiple Beat Bus Cycles
- Pipelining and Bursts
- Communication Channels

#### Agilent Technologies' Test and Measurement Support, Services, and Assistance

Agilent Technologies aims to maximize the value you receive, while minimizing your risk and problems. We strive to ensure that you get the test and measurement capabilities you paid for and obtain the support you need. Our extensive support resources and services can help you choose the right Agilent products for your applications and apply them successfully. Every instrument and system we sell has a global warranty. Support is available for at least five years beyond the production life of the product. Two concepts underlay Agilent's overall support policy: "Our Promise" and "Your Advantage."

#### **Our Promise**

Our Promise means your Agilent test and measurement equipment will meet its advertised performance and functionality. When you are choosing new equipment, we will help you with product information, including realistic performance specifications and practical recommendations from experienced test engineers. When you use Agilent equipment, we can verify that it works properly, help with product operation, and provide basic measurement assistance for the use of specified capabilities, at no extra cost upon request. Many self-help tools are available.

#### Your Advantage

Your Advantage means that Agilent offers a wide range of additional expert test and measurement services, which you can purchase according to your unique technical and business needs. Solve problems efficiently and gain a competitive edge by contracting with us for calibration, extra-cost upgrades, out-of-warranty repairs, and on-site education and training, as well as design, system integration, project management, and other professional services. Experienced Agilent engineers and technicians worldwide can help you maximize your productivity, optimize the return on investment of your Agilent instruments and systems, and obtain dependable measurement accuracy for the life of those products. By Internet, phone, or fax, get assistance with all your test and measurement needs

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